CLAIMS:

1. Linear phase detector for in response to at least one reference signal (REF) and at least a first (CLK-Q) and second (CLK-I) clock signal generating at least a first (UP) and second (DOWN) control signal and comprising at least a first circuit (1) receiving said reference signal (REF) and said first clock signal (CLK-Q) and a second circuit (2) receiving said reference signal (REF) and said second clock signal (CLK-I), wherein said first and second circuits (1,2) each comprise at least two latches (10,11,20,21) and at least one multiplexer (12,22) for multiplexing latch output signals, with said linear phase detector comprising a third circuit (3) for generating at least one of said control signals (UP,DOWN).

2. Linear phase detector according to claim 1, wherein said third circuit (3) comprises a latch (30) receiving said first (CLK-Q) and second (CLK-I) clock signal and generating said first control signal (UP), with one of the latches (20) of the second circuit (2) generating the second control signal (DOWN).

3. Linear phase detector according to claim 2, wherein said reference signal (REF) is supplied to at least one control input of said multiplexers (12,22) and to clock inputs of said latches (10,11,20,21) of said first (1) and second (2) circuits, with said first clock signal (CLK-Q) being supplied to at least one data input of said latches (10,11) of said first circuit (1) and with said second clock signal (CLK-I) being supplied to at least one data input of said latches (20,21) of said second circuit (2).

4. Linear phase detector according to claim 1, wherein said third circuit (3) comprises first logical circuitry (31,32) receiving the latch output signals of said first circuit (1) for generating said first control signal (UP) and comprises second logical circuitry (33,34) receiving the latch output signals of said second circuit (2) for generating said second control signal (DOWN).

5. Linear phase detector according to claim 4, wherein said first logical circuitry (31,32) comprises at least a first (31) and second (32) EXOR gate, the first EXOR gate receiving said latch output signals from said first circuit (1), the second EXOR gate (32) receiving output signals from said first EXOR gate (31) and from a third EXOR gate (33) for generating said first control signal (UP), with said second logical circuitry (33,34) comprises at least said third (33) and a fourth (34) EXOR gate, the third EXOR gate (33) receiving said

latch output signals from said second circuit (2), the fourth EXOR gate (34) receiving output signals from said third EXOR gate (33) and from a source for generating said second control signal (DOWN).

6. Linear phase detector according to claim 5, wherein said first logical circuitry (31,32,35) comprises a fifth EXOR gate (35) receiving said output signals from said first EXOR gate (31) and from a source for balancing said third circuit (3).

7. Linear phase detector according to claim 6, wherein said reference signal is supplied to at least one control input of said multiplexers (12,22) and to clock inputs of said latches (10,11,20,21), with said first clock signal being supplied to at least one data input of said latches (10,11) of said first circuit (1) and with said second clock signal being supplied to at least one data input of said latches (20,21) of said second circuit (2).

8. Apparatus comprising a linear phase detector for in response to at least one reference signal (REF) and at least a first (CLK-Q) and second (CLK-I) clock signal generating at least a first (UP) and second (DOWN) control signal and comprising at least a first circuit (1) receiving said reference signal (REF) and said first clock signal (CLK-Q) and a second circuit (2) receiving said reference signal (REF) and said second clock signal (CLK-I), wherein said first and second circuits (1,2) each comprise at least two latches (10,11,20,21) and at least one multiplexer (12,22) for multiplexing latch output signals, with said linear phase detector comprising a third circuit (3) for generating at least one of said control signals (UP,DOWN).

9. Method for linearly phase detecting through in response to at least one reference signal (REF) and at least a first (CLK-Q) and second (CLK-I) clock signal generating at least a first (UP) and second (DOWN) control signal and comprising a first step of receiving said first clock signal (CLK-Q) and a second step of receiving said second clock signal (CLK-I) and a third step of receiving said reference signal (REF), wherein said method comprises a fourth step of latching said reference signal (REF) and one of said clock signals (CLK-Q) and of multiplexing latched signals and a fifth step of latching said reference signal (REF) and the other one of said clock signals (CLK-I) and of multiplexing latched signals and a sixth step of generating at least one of said control signals (UP,DOWN).

10. Processor program product for linearly phase detecting through in response to at least one reference signal (REF) and at least a first (CLK-Q) and second (CLK-I) clock signal generating at least a first (UP) and second (DOWN) control signal and comprising a first function of receiving said first clock signal (CLK-Q) and a second function of receiving said second clock signal (CLK-I) and a third function of receiving said reference signal (REF), wherein said processor program product comprises a fourth function of latching said reference signal (REF) and one of said clock signals (CLK-Q) and of multiplexing latched signals and a fifth function of latching said reference signal (REF) and the other one of said clock signals (CLK-I) and of multiplexing latched signals and a sixth function of generating at least one of said control signals (UP,DOWN).